

250mA, Low Quiescent Current, Ultra-Low Noise, High PSRR Low-Dropout Linear Regulator

FEATURES

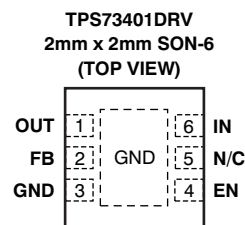
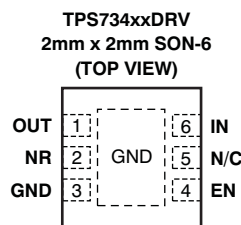
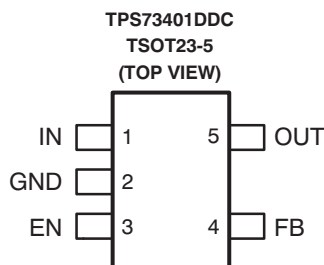
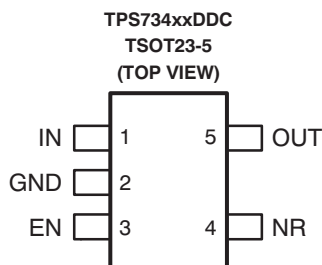
- 250mA Low Dropout Regulator with EN
- Low I_Q : 44 μ A
- Multiple Output Voltage Versions Available:
 - Fixed Outputs of 1.0V to 4.3V Using Innovative Factory EEPROM Programming
 - Adjustable Outputs from 1.25V to 6.2V
- High PSRR: 60dB at 1kHz
- Ultra-low Noise: 28 μ V_{RMS}
- Fast Start-Up Time: 45 μ s
- Stable with a Low-ESR, 2.0 μ F Typical Output Capacitance
- Excellent Load/Line Transient Response
- 2% Overall Accuracy (Load/Line/Temp)
- Very Low Dropout: 125mV at 250mA
- ThinSOT-23, 2mm x 2mm SON-6, and 3mm x 3mm SON-8 Packages

DESCRIPTION

The TPS734xx family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 44 μ A (typical) ground current. The TPS734xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 125mV at 250mA output. The TPS734xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ and is offered in low-profile ThinSOT-23, 2mm x 2mm SON, and 3mm x 3mm SON packages that are ideal for wireless handsets, printers, and WLAN cards.

APPLICATIONS

- WiFi, WiMax
- Printers
- Cellular Phones, SmartPhones
- Handheld Organizers, PDAs



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TPS734xxyyyzz	<p>XX is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable).</p> <p>YYY is package designator.</p> <p>Z is package quantity.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Output voltages from 1.0V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating temperature range (unless otherwise noted).

PARAMETER	TPS734xx	UNIT
V _{IN} range	-0.3 to +7.0	V
V _{EN} range	-0.3 to V _{IN} +0.3	V
V _{OUT} range	-0.3 to V _{IN} +0.3	V
V _{FB} range	-0.3 to V _{FB} (TYP) +0.3	V
Peak output current	Internally limited	
Continuous total power dissipation	See Dissipation Ratings Table	
Junction temperature range, T _J	-55 to +150	°C
Storage junction temperature range, T _{STG}	-55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = +25°C	T _A < +25°C	T _A = +70°C	T _A = +85°C
Low-K ⁽¹⁾	DDC	90°C/W	280°C/W	3.6mW/°C	360mW	200mW	145mW
High-K ⁽²⁾	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW
Low-K ⁽¹⁾	DRV	20°C/W	140°C/W	7.1mW/°C	715mW	395mW	285mW
High-K ⁽²⁾	DRV	20°C/W	65°C/W	15.4mW/°C	1.54W	845mW	615mW

- (1) The JEDEC low-K (1s) board used to derive this data was a 3in x 3in (7,62cm x 7,62cm), two-layer board with 2-ounce (56,699g) copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in (7,62cm x 7,62cm), multilayer board with 1-ounce (28,35g) internal power and ground planes and 2-ounce (56,699g) copper traces on top and bottom of the board

ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS73401, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range ⁽¹⁾		2.7		6.5	V
V_{FB}	Internal reference (TPS73401)		1.184	1.208	1.232	V
V_{OUT}	Output voltage range (TPS73401)		V_{FB}		6.3	V
V_{OUT}	Output accuracy	Nominal $T_J = +25^{\circ}\text{C}$	-1.0		+1.0	%
V_{OUT}	Output accuracy ⁽¹⁾	Over V_{IN} , I_{OUT} , Temp $V_{OUT} + 0.3\text{V} \leq V_{IN} \leq 6.5\text{V}$ $1\text{mA} \leq I_{OUT} \leq 250\text{mA}$	-2.0	± 1.0	+2.0	%
$\Delta V_{OUT}\% / \Delta V_{IN}$	Line regulation ⁽¹⁾	$V_{OUT(NOM)} + 0.3\text{V} \leq V_{IN} \leq 6.5\text{V}$		0.02		%/V
$\Delta V_{OUT}\% / \Delta I_{OUT}$	Load regulation	$500\mu\text{A} \leq I_{OUT} \leq 250\text{mA}$		0.005		%/mA
V_{DO}	Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(NOM)} - 0.1\text{V}$)	$I_{OUT} = 250\text{mA}$		125	219	mV
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	300	580	900	mA
I_{GND}	Ground pin current	$500\mu\text{A} \leq I_{OUT} \leq 250\text{mA}$		45	65	μA
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.4\text{V}$		0.15	1.0	μA
I_{FB}	Feedback pin current (TPS73401)		-0.5		0.5	μA
PSRR	Power-supply rejection ratio $V_{IN} = 3.85\text{V}$, $V_{OUT} = 2.85\text{V}$, $C_{NR} = 0.01\mu\text{F}$, $I_{OUT} = 100\text{mA}$	$f = 100\text{Hz}$		60		dB
		$f = 1\text{kHz}$		56		dB
		$f = 10\text{kHz}$		41		dB
		$f = 100\text{kHz}$		28		dB
V_N	Output noise voltage BW = 10Hz to 100kHz, $V_{OUT} = 2.8\text{V}$	$C_{NR} = 0.01\mu\text{F}$		$11 \times V_{OUT}$		μV_{RMS}
		$C_{NR} = \text{none}$		$95 \times V_{OUT}$		μV_{RMS}
T_{STR}	Startup time, $V_{OUT} = 0 \sim 90\%$, $V_{OUT} = 2.85\text{V}$, $R_L = 14\Omega$, $C_{OUT} = 2.2\mu\text{F}$	$C_{NR} = \text{none}$		45		μs
		$C_{NR} = 0.001\mu\text{F}$		45		μs
		$C_{NR} = 0.01\mu\text{F}$		50		μs
		$C_{NR} = 0.047\mu\text{F}$		50		μs
$V_{EN(HI)}$	Enable high (enabled)		1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)		0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	$V_{EN} = V_{IN} = 6.5\text{V}$		0.03	1.0	μA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		$^{\circ}\text{C}$
		Reset, temperature decreasing		145		$^{\circ}\text{C}$
T_J	Operating junction temperature		-40		+125	$^{\circ}\text{C}$
UVLO	Undervoltage lock-out	V_{IN} rising	1.90	2.20	2.65	V
	Hysteresis	V_{IN} falling		70		mV

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V , whichever is greater.

(2) V_{DO} is not measured for devices with $V_{OUT(NOM)} < 2.8\text{V}$ because minimum $V_{IN} = 2.7\text{V}$.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

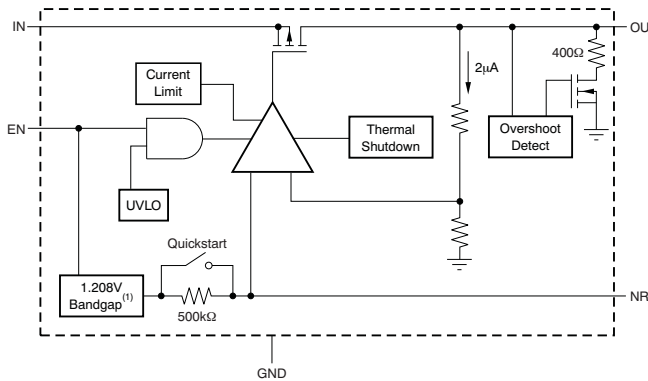


Figure 1. Fixed Voltage Versions

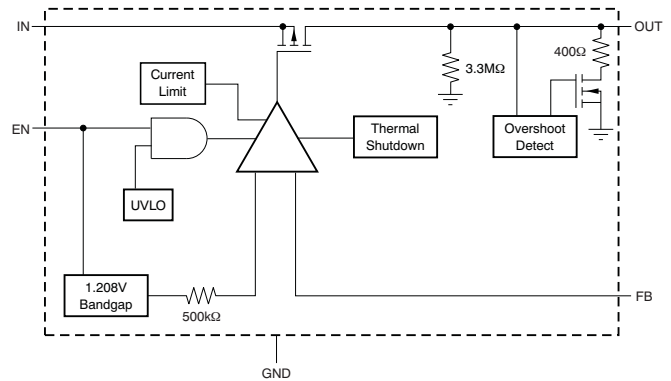
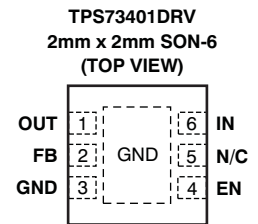
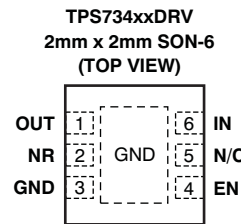
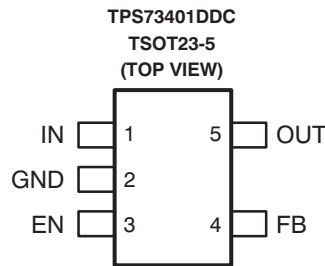
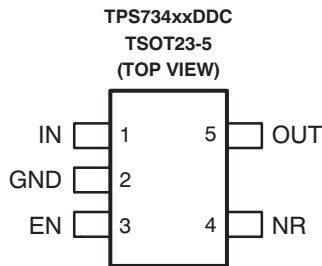


Figure 2. Adjustable Voltage Versions

NOTE (1): Fixed voltage versions between 1.0V to 1.2V have a 1.0V bandgap circuit instead of a 1.208V bandgap circuit.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

TPS734xx				DESCRIPTION
NAME	DDC	DRV	DRB	
IN	1	6	8	Input supply.
GND	2	3, Pad	4	Ground. The pad must be tied to GND.
EN	3	4	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	2	3	Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	4	2	3	Adjustable version only; this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	1	1	Output of the regulator. A small capacitor (total typical capacitance $\geq 2.0\mu\text{F}$ ceramic) is needed from this pin to ground to assure stability.
N/C	—	5	2, 6, 7	Not internally connected. This pin must either be left open, or tied to GND.

TYPICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$); $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS73401, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

TPS73401 LINE REGULATION

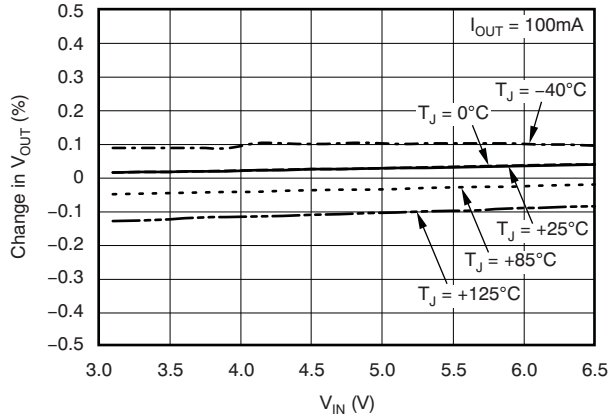


Figure 3.

TPS73425 LINE REGULATION

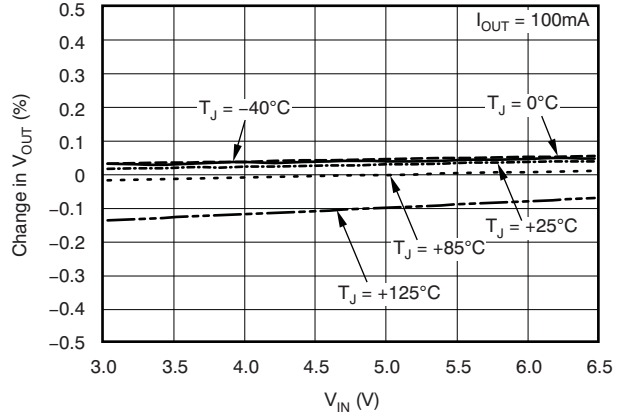


Figure 4.

TPS73401 LOAD REGULATION

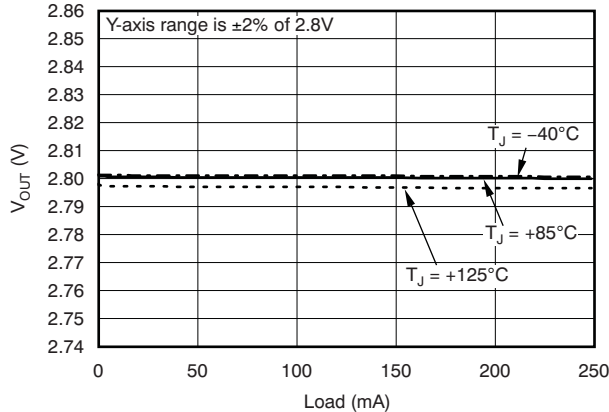


Figure 5.

TPS73425 LOAD REGULATION

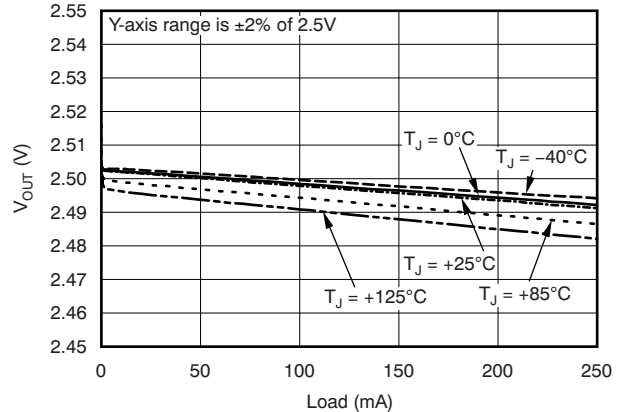


Figure 6.

TPS73425 GROUND PIN CURRENT vs OUTPUT CURRENT

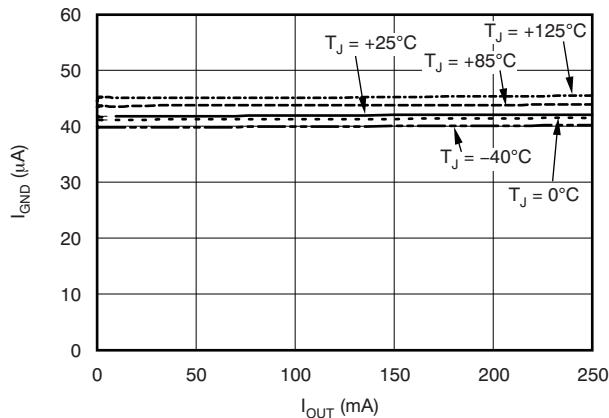


Figure 7.

TPS73425 GROUND PIN CURRENT (DISABLE) vs TEMPERATURE

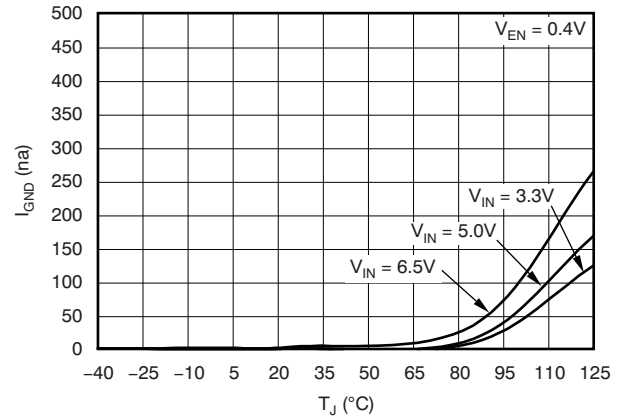


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$); $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS73401, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

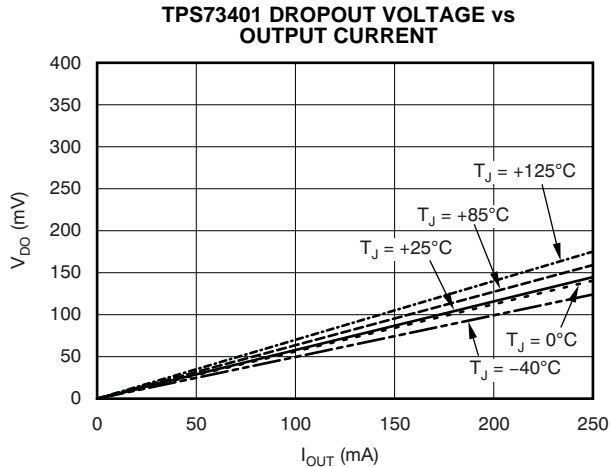


Figure 9.

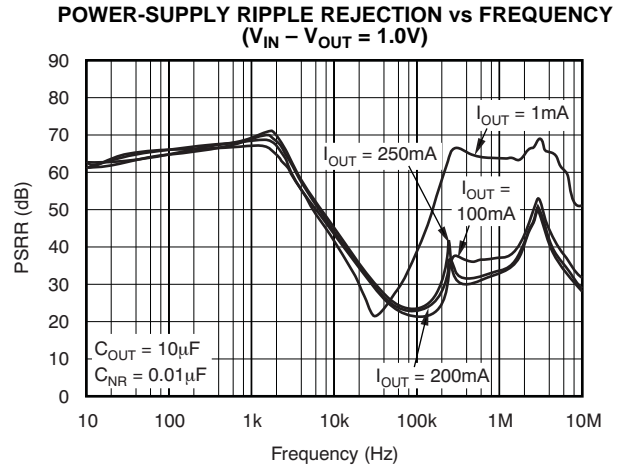


Figure 10.

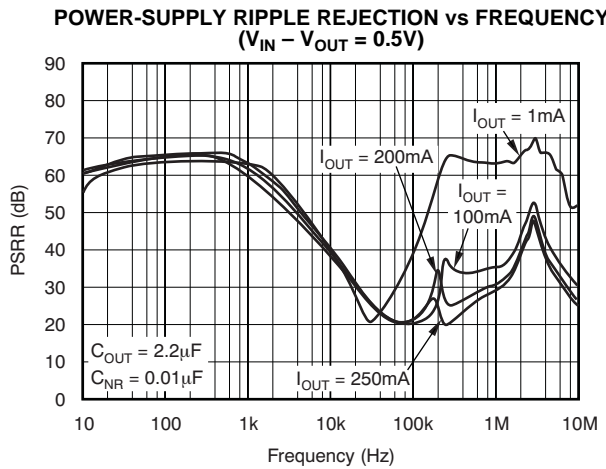


Figure 11.

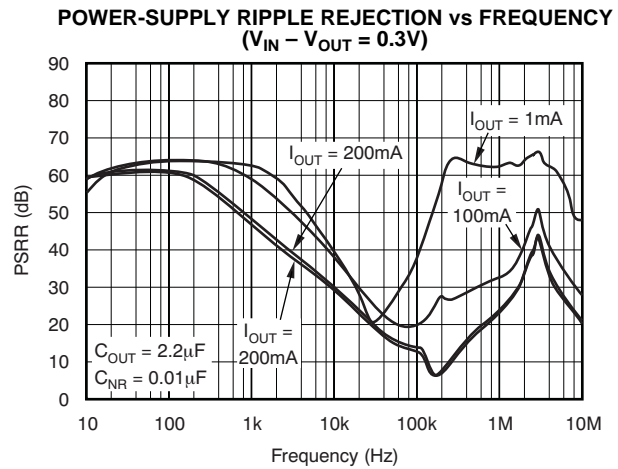


Figure 12.

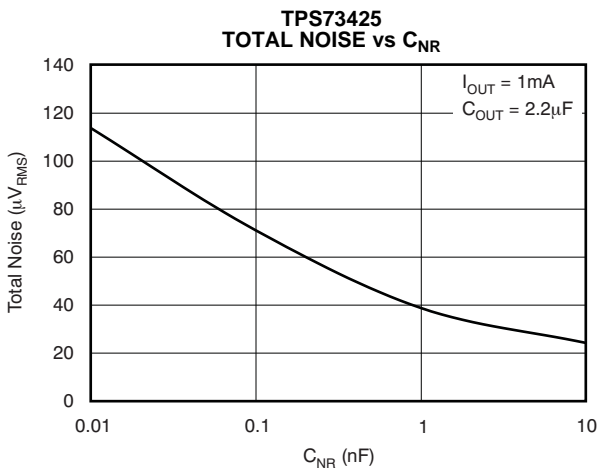


Figure 13.

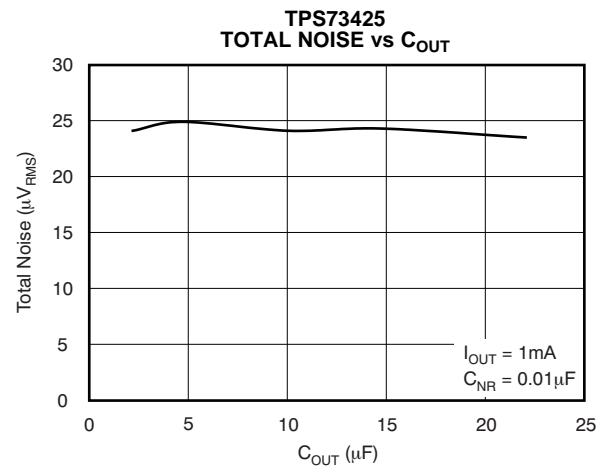


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$); $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$ or 2.7V , whichever is greater; $I_{OUT} = 1\text{mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$, unless otherwise noted. For TPS73401, $V_{OUT} = 3.0\text{V}$. Typical values are at $T_J = +25^{\circ}\text{C}$.

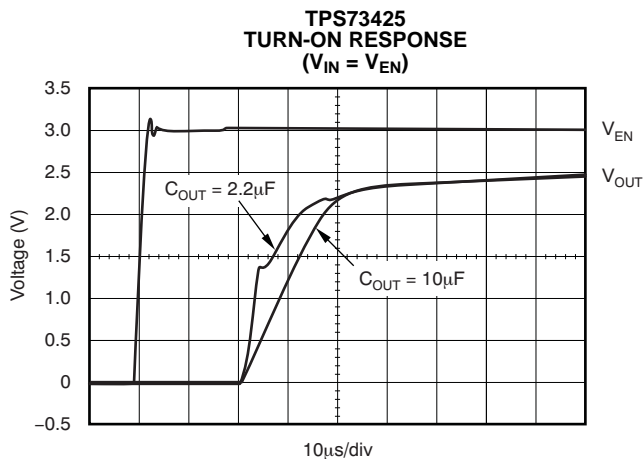


Figure 15.

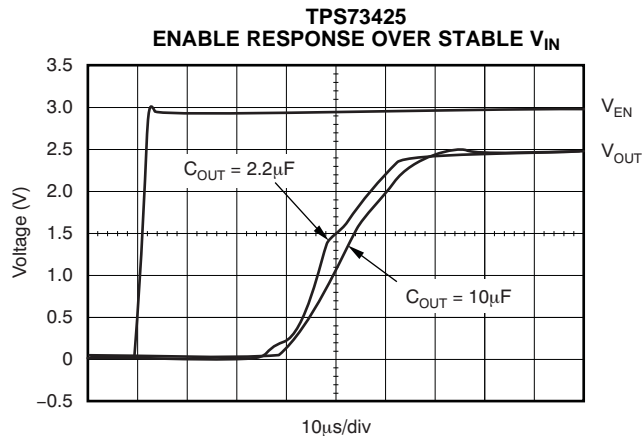


Figure 16.

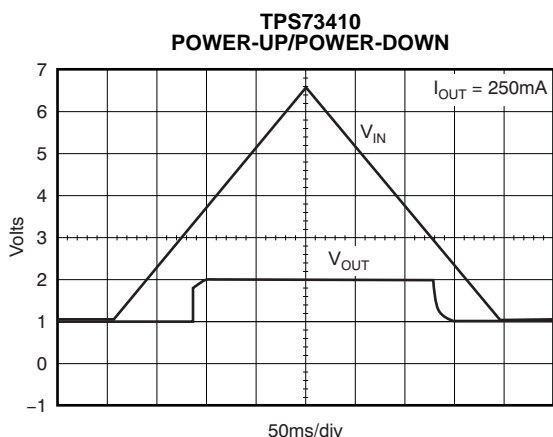


Figure 17.

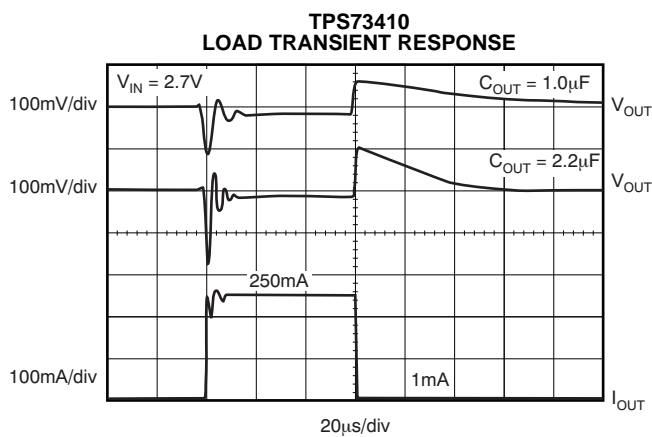


Figure 18.

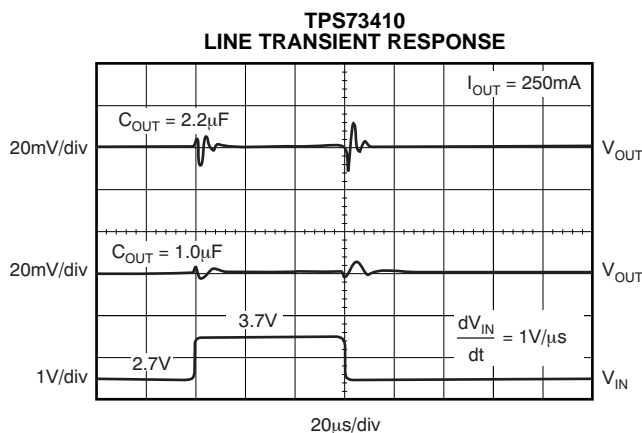


Figure 19.

APPLICATION INFORMATION

The TPS734xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom ($V_{IN} - V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS734xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from -40°C to $+125^{\circ}\text{C}$.

Figure 20 shows the basic circuit connections for fixed voltage models. Figure 21 gives the connections for the adjustable output version (TPS73401). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 21.

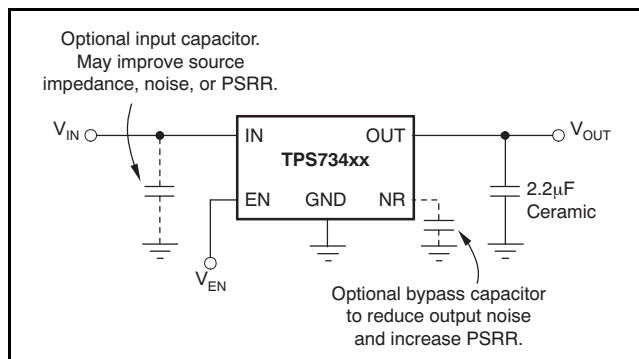


Figure 20. Typical Application Circuit for Fixed Voltage Versions

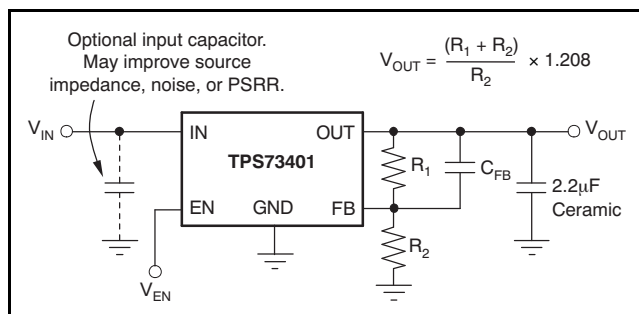


Figure 21. Typical Application Circuit for Adjustable Voltage Versions

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a $0.1\mu\text{F}$ to $1\mu\text{F}$ low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ground of this capacitor should be connected as close as the ground of output capacitor; a capacitor value of $0.1\mu\text{F}$ is enough in this condition. When it is difficult to place these two ground points close together, a $1\mu\text{F}$ capacitor is recommended. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a $0.1\mu\text{F}$ input capacitor may be necessary to ensure stability.

The TPS734xx is designed to be stable with standard ceramic output capacitors of values $2.2\mu\text{F}$ or larger. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor should be $< 1.0\Omega$, so output capacitor type should be either ceramic or conductive polymer electrolytic.

Feedback Capacitor Requirements (TPS73401 only)

The feedback capacitor, C_{FB} , shown in Figure 21 is required for stability. For a parallel combination of R_1 and R_2 equal to $250\text{k}\Omega$, any value from 3pF to 1nF can be used. Fixed voltage versions have an internal 30pF feedback capacitor that is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5pF should be used to ensure fast startup; values above 47pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS73401 is stable in unity-gain configuration (OUT tied to FB) without C_{FB} .

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS734xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a $0.01\mu\text{F}$ noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives $2\mu\text{A}$ of divider current has the same noise performance as a fixed voltage version. To further

optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω . This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with $C_{NR} = 0.01\mu\text{F}$, total noise is given approximately by [Equation 1](#):

$$V_N = \frac{11\mu\text{V}_{\text{RMS}}}{V} \times V_{\text{OUT}} \quad (1)$$

The TPS73401 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS734xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS734xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS734xx uses a PMOS pass transistor to achieve low dropout. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{\text{DS, ON}}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with output current.

As with any linear regulator, PSRR and transient response are degraded as $(V_{\text{IN}} - V_{\text{OUT}})$ approaches dropout. This effect is shown in the [Typical Characteristics](#) section.

Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS734xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR} , if present (see the [Functional Block Diagrams](#)). This architecture allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to the [Typical Characteristics](#) section. The quick-start switch is closed for approximately $135\mu\text{s}$. To ensure that C_{NR} is fully charged during the quick-start time, a $0.01\mu\text{F}$ or smaller capacitor should be used.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB improves stability and transient response. The transient response of the TPS734xx is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400Ω resistor to ground.

Undervoltage Lock-Out (UVLO)

The TPS734xx utilizes an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than $50\mu\text{s}$ duration.

Minimum Load

The TPS734xx is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 1mA is required. Below 1mA at junction temperatures near $+125^\circ\text{C}$, the output can drift up enough to cause the output pull-down to turn on. The output pull-down limits voltage drift to 5% typically but ground current could increase by approximately $50\mu\text{A}$. In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current would then be valid at no load conditions in most applications.

Thermal Information

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS734xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS734xx into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Dissipation Ratings](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

Package Mounting

Solder pad footprint recommendations for the TPS734xx are available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73401DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCW	Samples
TPS73401DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCW	Samples
TPS73401DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CBG	Samples
TPS73401DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CBG	Samples
TPS73418DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CBI	Samples
TPS73418DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CBI	Samples
TPS73428DRVR	PREVIEW	WSON	DRV	6		TBD	Call TI	Call TI			
TPS73428DRVT	PREVIEW	WSON	DRV	6		TBD	Call TI	Call TI			
TPS73430DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVW	Samples
TPS73430DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVW	Samples
TPS73433DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OEV	Samples
TPS73433DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OEV	Samples
TPS73433DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVX	Samples
TPS73433DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVX	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73401DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73401DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73401DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73401DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73418DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73418DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73430DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73430DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73430DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS73430DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73433DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73433DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73433DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73433DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

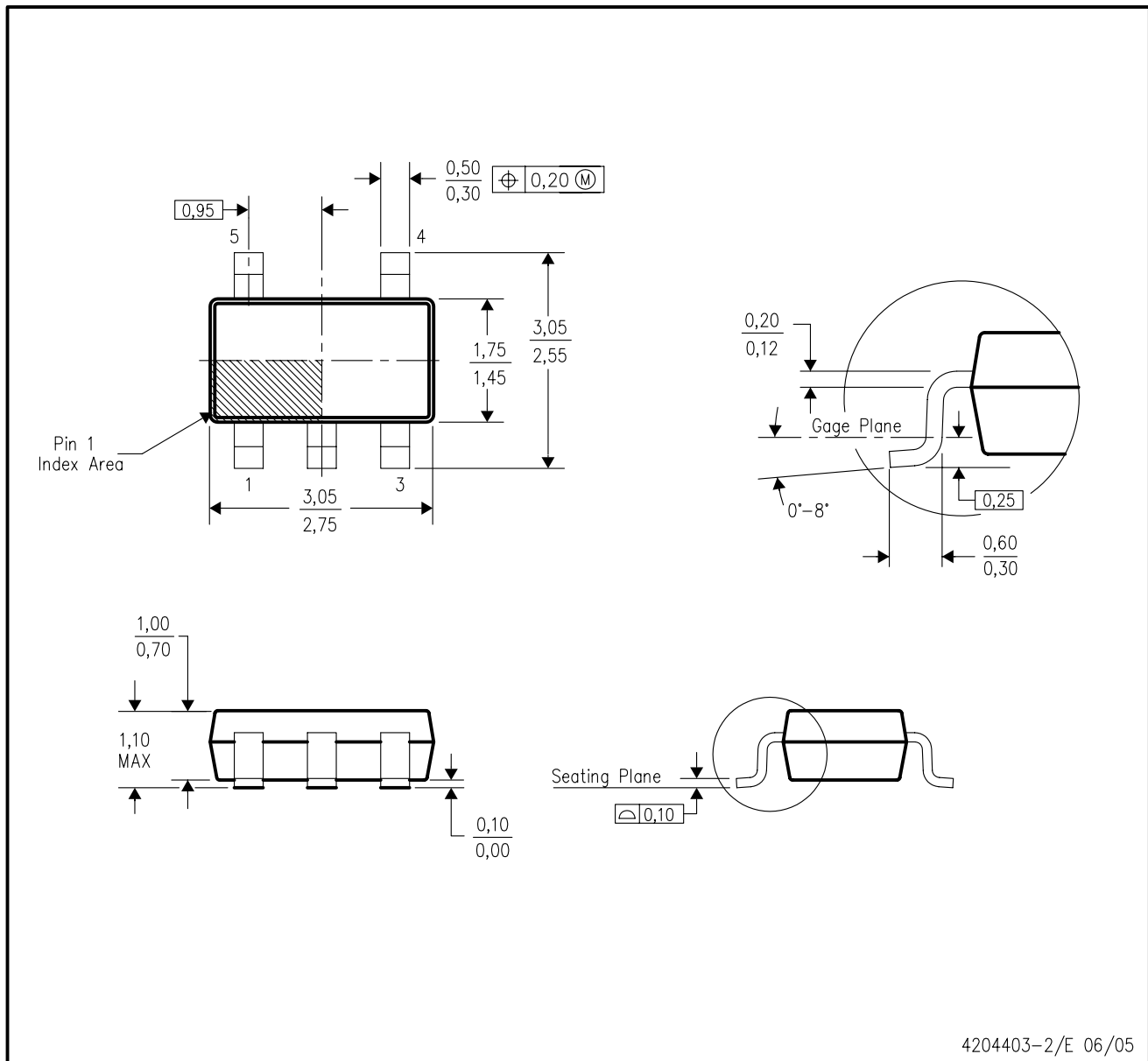
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73401DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS73401DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS73401DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS73401DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73418DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS73418DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73430DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS73430DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS73430DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS73430DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS73433DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS73433DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS73433DRVR	WSON	DRV	6	3000	203.0	203.0	35.0
TPS73433DRVT	WSON	DRV	6	250	203.0	203.0	35.0

DDC (R-PDSO-G5)

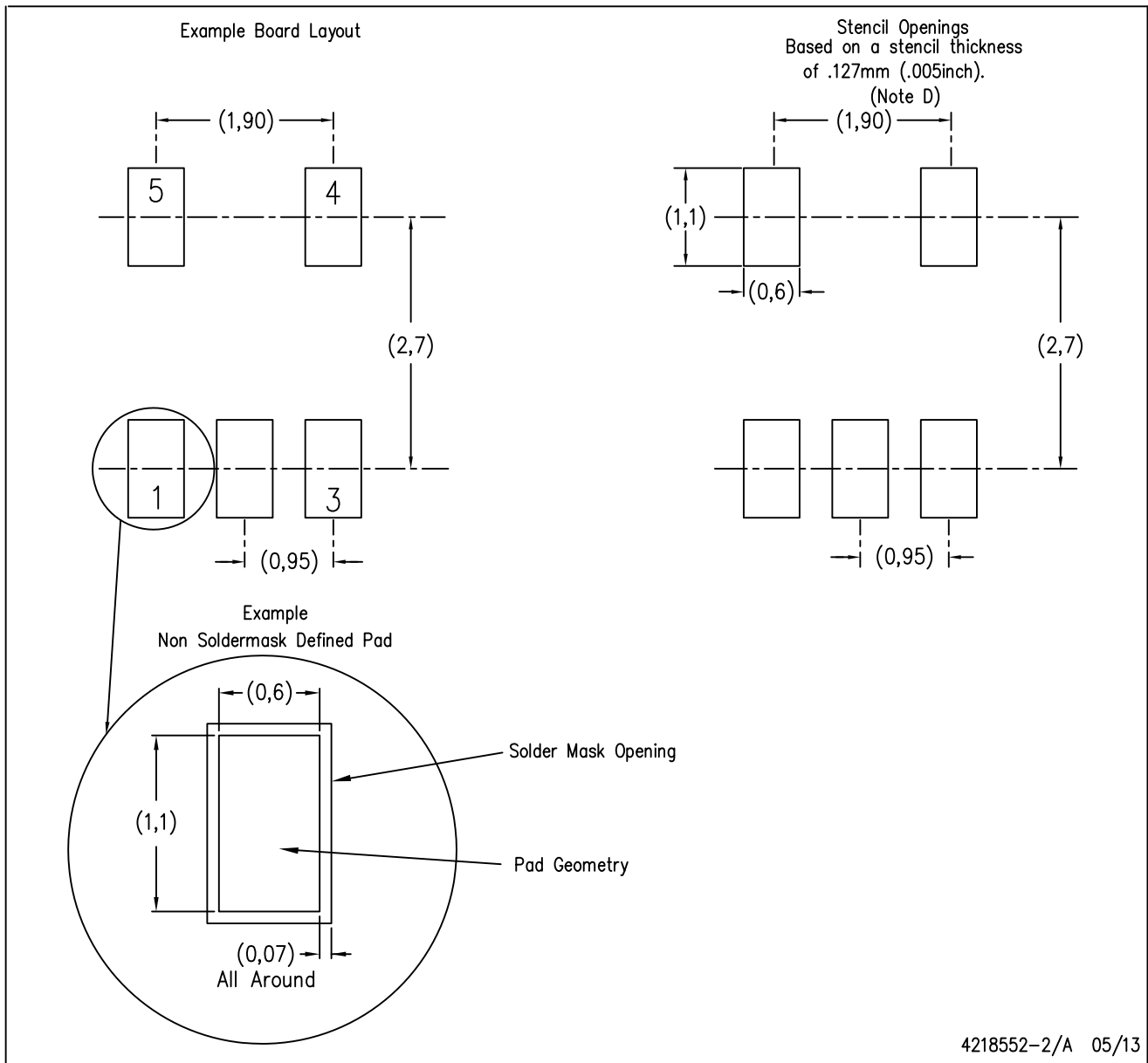
PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-193 variation AB (5 pin).

DDC (R-PDSO-G5)

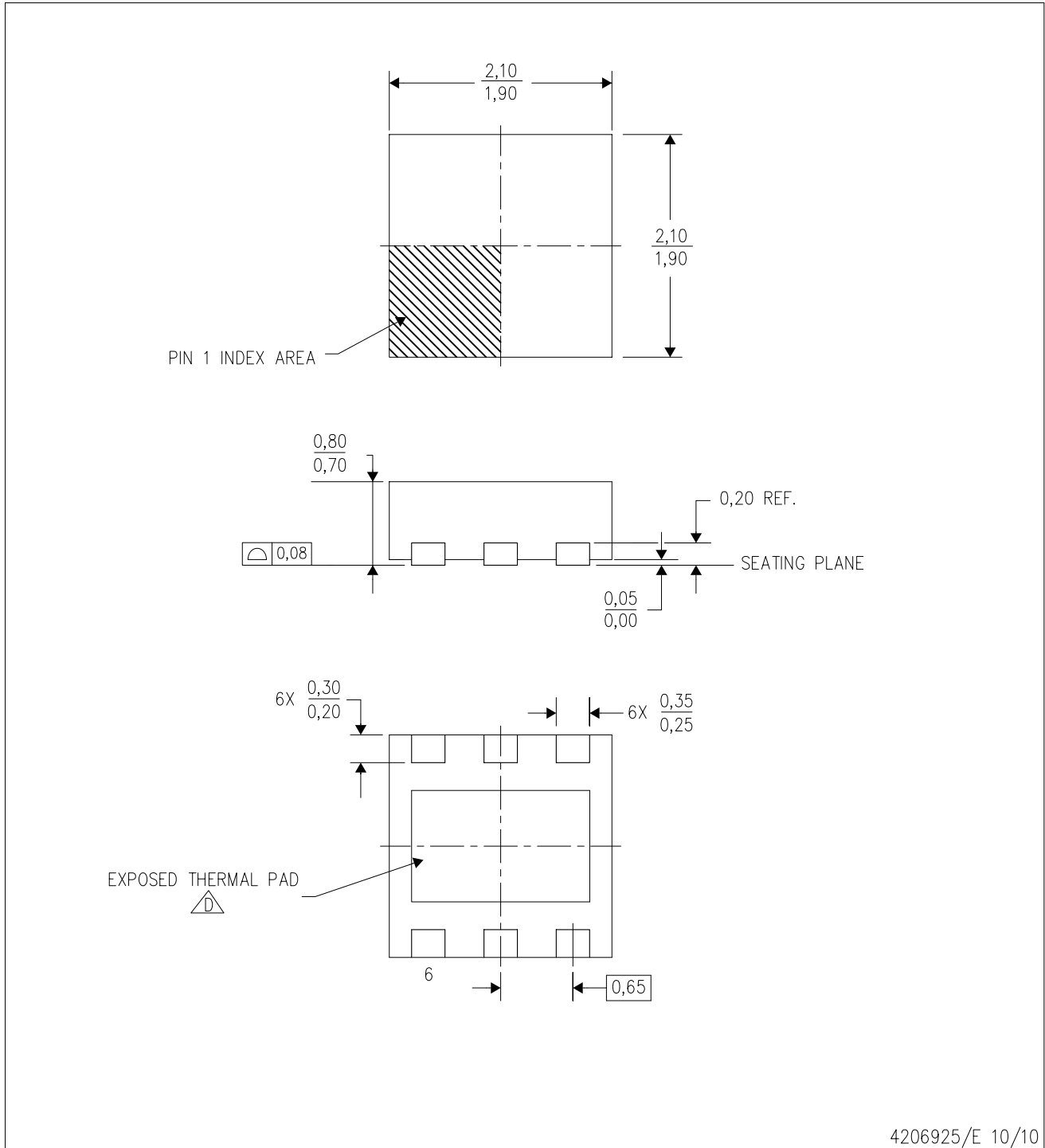
PLASTIC SMALL OUTLINE




- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

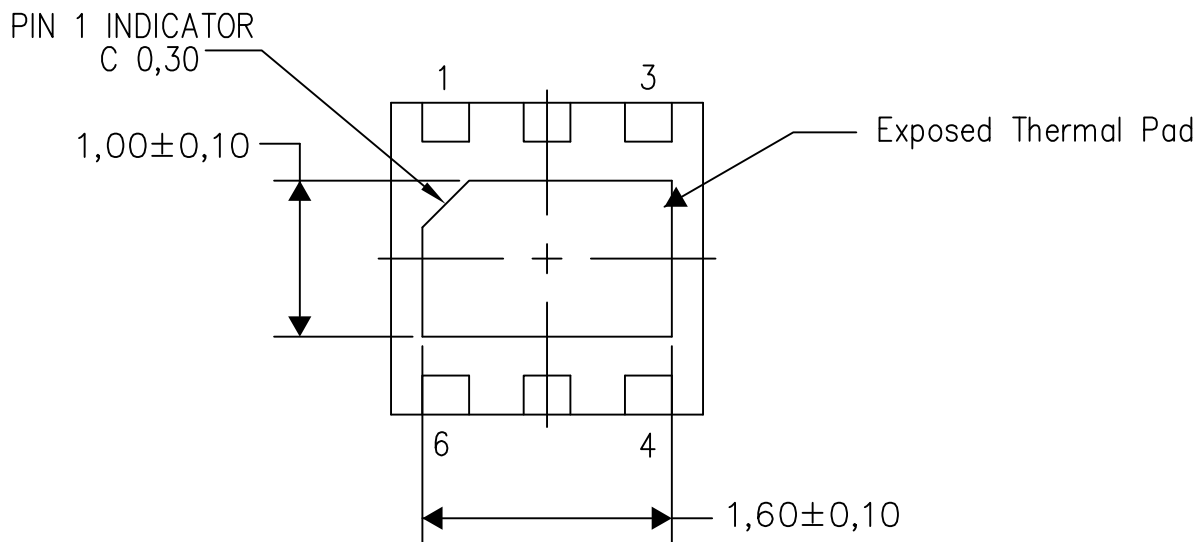
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

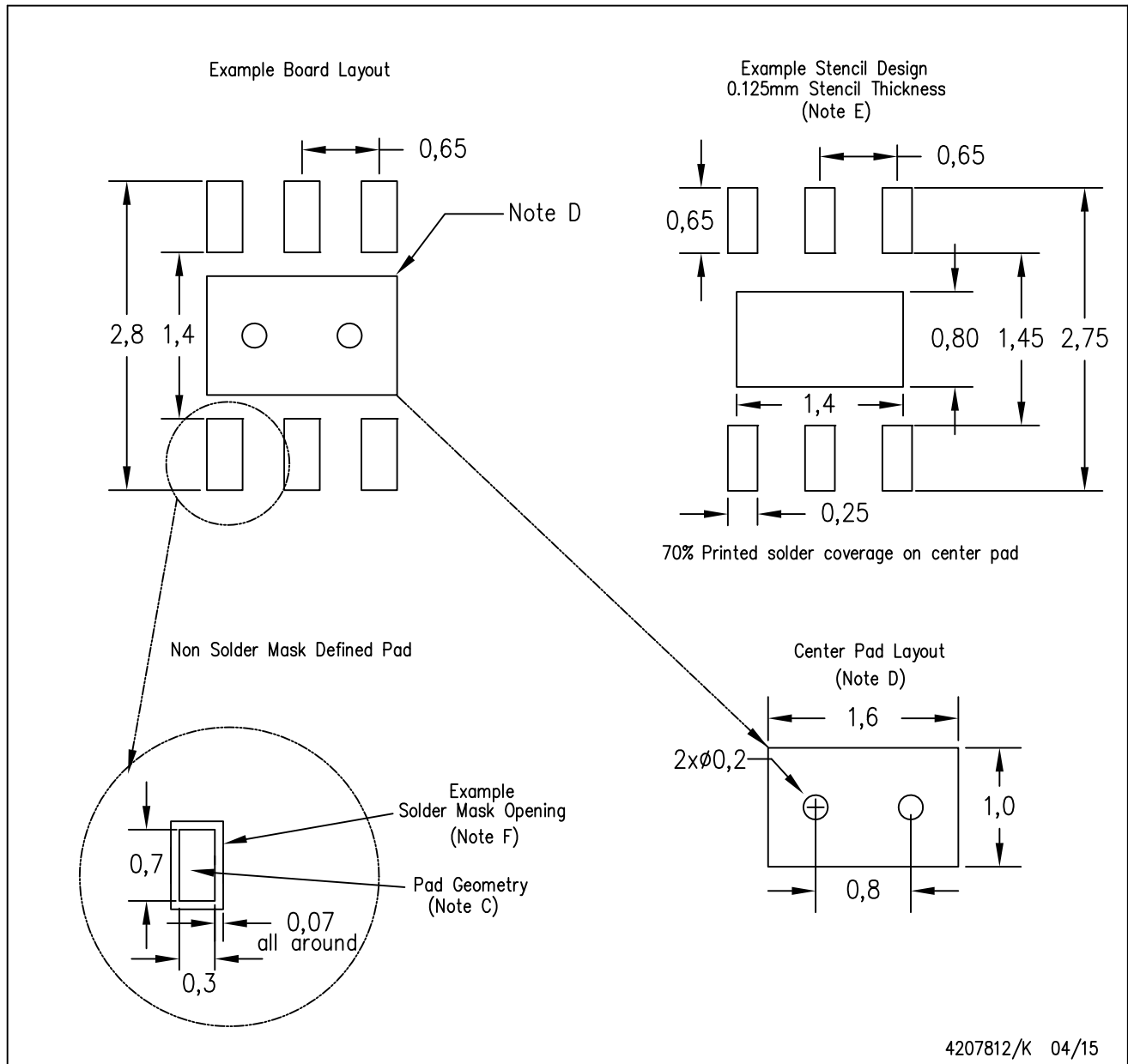
Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com